It is well known that word line drivers and sense amplifiers are responsive to separate addresses and thus should be isolated electrically from each other for proper memory operation.

Claim 1 has been rejected under 35 U. S. C. § 102(b) as being anticipated by U.S. patent 6,147,925 (Tomishima). The rejection is stated at paragraph 6 of the Office Action. It is submitted, however, that Tomishima lacks a disclosure of requirements of claim 1, which is reproduced, *inter alia*, as follows:

> 1. A semiconductor memory device, comprising:
>
> . . .
>
> a sense amplifier driving line provided in common to said plurality of sense amplifiers, and
>
> . . .
>
> said third transistor has a control terminal receiving an activation timing control signal for said sub-amplifier, and a second conductive terminal connected to said sense amplifier driving line.

This specifically required circuit configuration is illustrated, for example, by Figs. 2 and 3. As shown, the source of N-channel MOS transistor 103 is connected to sense amplifier driving line S2N (described at page 9, lines 10-11, of the specification).

Tomishima discloses a control system of isolation transistors (isolation gates) arranged between bit lines connecting to a plurality of memory cells and sense amplifiers corresponding to the bit lines. Specifically, the control system enables the sense operation faster by making the resistance of the on-state isolation transistors high, which leads to the substantial isolation of the bit lines' load capacitance viewed from the sense amplifiers. As described above, Tomishima does not disclose a sub-amplifier equivalent to the sub-amplifier disclosed in the present application to define claim 1.

The Office Action equates the configuration shown in Figs. 21 and 30 of Tomishima with the arrangement shown in Figs. 2 and 3 of the present application. However, "Si" shown in Fig. 21 of Tomishima is not a sense amplifier driving line as defined by the present disclosure. In addition,

with respect to Fig. 30 of Tomishima, "SVC" shown in Fig. 30, which apparently has been held to correspond to sense amplifier driving line S2N shown in Fig. 3 in the present application, is merely a source power supply line connected to the node of power supply voltage Vcc, not a sense amplifier driving line.

Furthermore, Tomishima does not teach or suggest the effect of claim 1 that sub-amplifier 100 can be operated only when the row block adjacent to one of sense amplifier zones 3 is activated, without adding a circuit configuration for supplying a signal notifying of activation of the row block (as described at page 9, lines 21-24 of the specification).

Accordingly, it is submitted that claim 1 is patentably distinguishable from Tomishima. Allowance of the application is respectfully solicited. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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